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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,609	01/16/2004	Tetsumasa Sato	60675 (48229)	8169

7590 02/08/2005

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EXAMINER	
HO, TU TU V	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,609	SATO, TETSUMASA	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *8-15,17-19 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,16,20 and 22* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 06/22/2004 is acceptable.

Election/ Restriction

2. Applicant's election of Invention I, **claims 1-7, 16, 20 and 22**, in the reply filed on 01/10/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

3. **Claims 8-15, 17-19, and 21** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 01/10/2005 as noted above.

Drawings

4. **Figures 28-34** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not

accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. **Claim 16** is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim can not depend from any other multiple dependent claim. See MPEP § 608.01(n). In particular, claims 4-5 and 12 are multiple dependent claims (claim 5 depends on claim 4, which depends on claim 3, which is a multiple dependent claim, making claims 4 and 5 multiple dependent). Furthermore, since claims 8-15, 17-19, and 21 are withdrawn from consideration, for examination purpose, claim 16 in interpreted as "The manufacturing method of the semiconductor device according to any one of the claims 1, 2, 6, or 7, wherein the element isolation region is semi-recessed LOCOS".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-7 and 20** are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda et al. U.S. Patent 4,898,837 (the '837 patent).

The '837 patent discloses in Figures 2's through 6's, particularly Figs. 2H and 6B, and respective portions of the specification a manufacturing method of a semiconductor device as claimed.

Referring to **claim 1**, the '837 patent discloses a manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region (generally defined by 24, column 4, lines 31-35) and an active region (generally defined by 28, column 4, lines 48-52), electrically isolated by the element isolation region, on a semiconductor layer (23); and

(b) forming a resistive impurity layer (28, Fig. 2D), at least, in a part of the active region by forming a first impurity-doping region, and providing a first impurity-doping forbidden region (26, 27) in the element isolation region at the same time.

Referring to **claims 3-4 and 6** and using the same reference characters and citations as detailed above for claim 1 where applicable, the reference discloses a manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region and an active region, electrically isolated by the element isolation region, on a semiconductor layer;

(b) forming a resistive impurity layer, at least, in a part of the active region by forming a first impurity-doping region; and

(c) forming a contact impurity layer (generally defined by 32, column 5, lines 5-10) by forming a second impurity-doping region (32) in a region, continuously connected to the resistive impurity layer, and providing a second impurity-doping forbidden region (30, Figs. 2F and 6B), at least, in the element isolation region at the same time.

Referring to **claim 2**, the reference further discloses that that a plurality of the resistive impurity layers (Figs. 6) are formed, and the first impurity-doping forbidden region (24) is formed so as to isolate the adjacent first impurity-doping regions in the (b).

Referring to **claims 5 and 7**, the reference further discloses that that a plurality of the contact impurity layers (Fig. 6, contact areas 32 and the two terminal sections of layer 29a, which terminal sections are connected to electrodes 35e, meeting the definitions of contacts) are formed, and the second impurity-doping forbidden region is formed so as to isolate, at least, the adjacent second impurity-doping regions

Referring to **claim 20**, the reference's disclosure of p-type impurity doping (column 4, lines 31-35) meets the requirement of the Markush group of the claim.

7. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by Usuki U.S. Patent 5,377,140.

Usuki discloses in Figure 12 a manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region ("field oxide film" 52, column 8, lines 10-14) and an active region (generally defined by 55/56), electrically isolated by the element isolation region, on a semiconductor layer (51); and

(b) forming a resistive impurity layer (55 or 56, column 8, lines 10-31), at least, in a part of the active region by forming a first impurity-doping region, and providing a first impurity-doping forbidden region ("resist mask" 57, column 8, lines 24-26) in the element isolation region at the same time.

8. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by Lasky U.S. Patent 5,888,875.

Lasky discloses in Figure 3 a manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region ("STI" 16, column 5, lines 48-52) and an active region (generally defined by 14), electrically isolated by the element isolation region, on a semiconductor layer (12); and

(b) forming a resistive impurity layer (diffusion area 14, column 5, lines 48-58), at least, in a part of the active region by forming a first impurity-doping region, and providing a first impurity-doping forbidden region ("diffusion barrier" 18, column 5, lines 48-58) in the element isolation region at the same time.

Claim Rejections § 102 & § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claim 22** is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the '837 patent.

The '837 patent discloses a manufacturing method of a semiconductor device as claimed and as detailed above including forming the contact impurity layer (32 or terminal parts of 29a) with a concentration of impurity and forming the resistive impurity layer 28 or 29a with a concentration of impurity, but fails to explicitly discloses that said contact impurity layer has a higher concentration of impurity than said resistive impurity layer. Nevertheless, the reference teaches in column 5 first full paragraph and column 7, lines 55-64, that impurity concentration for the contact areas is chosen such that it is suitable for forming contact low resistance characteristics. It appears that to obtain the low resistance characteristics, it is necessary to provide a higher concentration of impurity as claimed.

Claim Rejections - 35 USC § 103

10. **Claim 16** is rejected under 35 U.S.C. §103(a) as being unpatentable over the '837 patent in view of Hoover et al. U.S. Patent 5,798,295 (the '295 patent).

The '837 patent discloses a manufacturing method of a semiconductor device substantially as claimed and as detailed above including forming the resistive impurity layer and the element isolation region 24 for electrically isolating the resistive impurity layer. However, the reference fails to disclose that the element isolation region is semi-recessed LOCOS. The '295 patent, in also disclosing a manufacturing method of a semiconductor device including forming a resistive impurity layer 44 and the element isolation region 12 (Fig. 7) for electrically isolating the resistive impurity layer, teaches that element isolation region 12 could be formed by a LOCOS process or others such as trench isolation or alike (column 3, last paragraph). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention

was made to form the reference's isolation region as a semi-recessed LOCOS isolation region. One would have been motivated to make such a change because LOCOS or semi-recessed LOCOS or trench or other isolation regions is one of various types of isolation regions one of ordinary skill in the art would chose to form element isolation regions.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
January 31, 2005